European Commission

**MNEMOSENE** has received funding from the European Union's Horizon 2020 research and innovation programme under the ICT-31-2017 RIA grant agreement No 780215

# MNEMOSENE

www.mnemosene.eu

## Computation-in-Memory Architecture based on Resistive Devices

TU Delft · RWTH Aachen University · ETH zürich · IBM Research · TU/e Technische Universiteit Eindhoven University of Technology · Inria Inventeurs du monde numérique · imec · arm · intelligentsia consultants

# Rationale

Emerging applications (e.g. Big Data, IoT) are extremely demanding in terms of storage and computing power and have surpassed the capabilities of today's computation architectures and device technologies.

**Computer architecture walls:**

- Memory wall
- Instruction Level Parallelism (ILP) wall
- Energy wall

**CMOS technology walls:**

- Reliability wall
- Leakage wall
- Cost wall

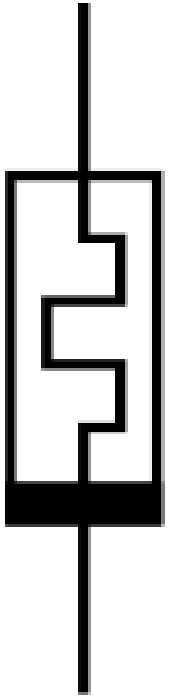
→ **Alternative computing architectures** and **emerging device technologies** need to be explored

European Commission

**MNEMOSENE** has received funding from the European Union's Horizon 2020 research and innovation programme under the ICT-31-2017 RIA grant agreement No 780215

# Memristors

Among emerging devices, **memristors** are promising candidates to complement and/or replace traditional CMOS. Current technological implementations present remarkable properties (although with strong trade-offs), which may include:



- CMOS process compatibility
- Relative low cost
- Zero standby power
- Nanosecond switching speed
- Enhanced scalability
- High density
- High OFF/ON resistance ratio
- Good endurance and retention time

More importantly, the memristor is a **two-terminal resistive-switching device** that can be used to build **both non-volatile storage and information processing**, thus enabling new computing paradigms

European Commission

**MNEMOSENE** has received funding from the European Union's Horizon 2020 research and innovation programme under the ICT-31-2017 RIA grant agreement No 780215

# Overall Objective

**MNEMOSENE** aims at demonstrating a new architecture concept together with its required programming flow and interface. The project's overall goal is twofold:

- **Develop, design and demonstrate the concept of computation-in-memory (CIM)** based on resistive-computing using emerging non-volatile memresistive switching devices.

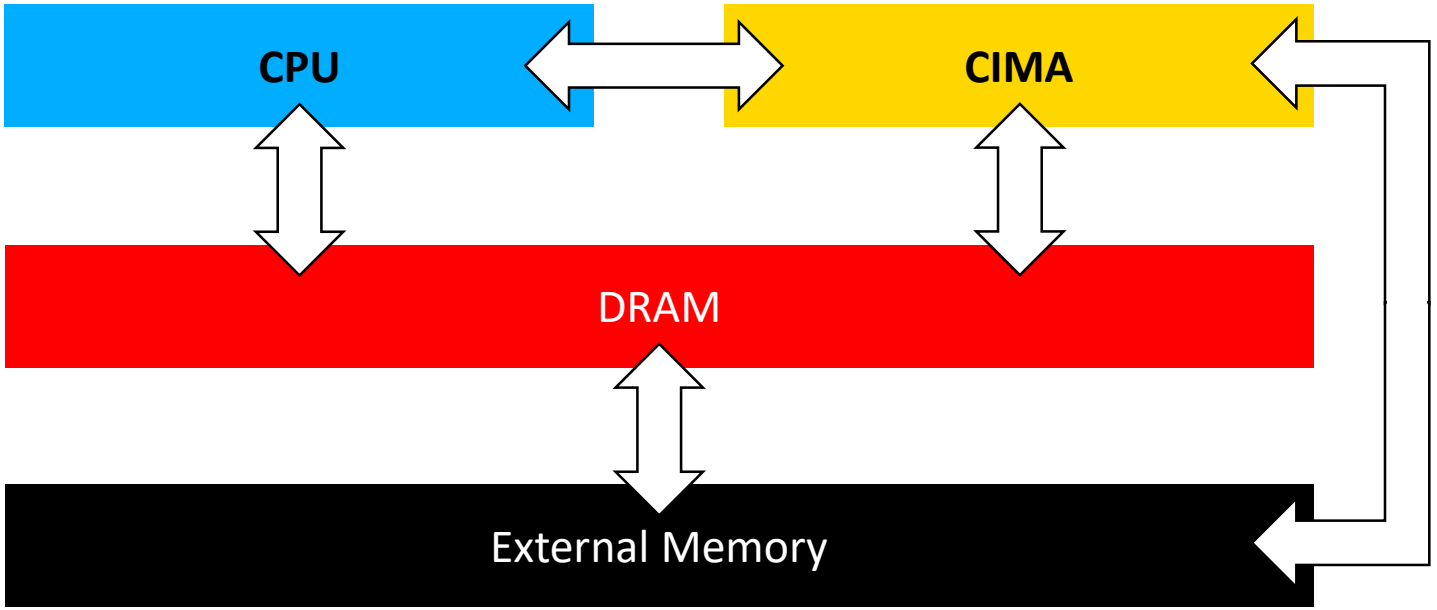
- **Develop and design a simulator and FPGA emulator for the new architecture** (CIM device combined with a conventional CPU).

Additionally, a particular focus will be placed on the **evaluation of the trade-offs for different memristor technological implementations**, in consideration of the requirements of specific applications.

European Commission

**MNEMOSENE** has received funding from the European Union's Horizon 2020 research and innovation programme under the ICT-31-2017 RIA grant agreement No 780215

# Overall Objective




Integrating the processing units and the memory in the same physical location allows for the working set of the most memory accessing part of an application to be moved into the CIM core (rather than DRAM or cache).

European Commission

**MNEMOSENE** has received funding from the European Union's Horizon 2020 research and innovation programme under the ICT-31-2017 RIA grant agreement No 780215

# Scientific and Technical Objectives

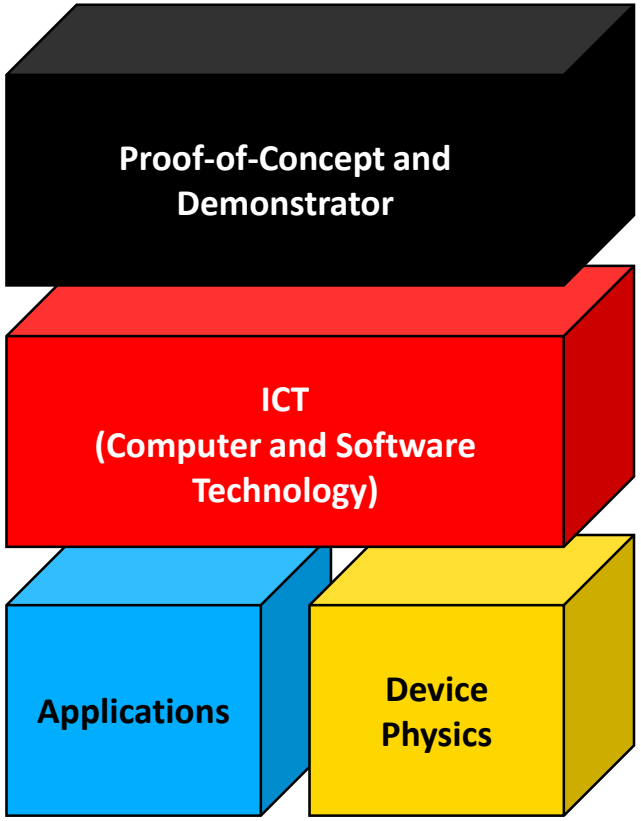
- **Objective 1**: Develop new algorithmic solutions for targeted applications for CIM architecture.
- **Objective 2**: Develop and design new mapping methods integrated in a framework for efficient compilation of the new algorithms into CIM macro-level operations.
- **Objective 3**: Develop a macro-architecture based on the integration of group of CIM tiles.
- **Objective 4**: Develop and demonstrate the micro-architecture level of CIM tiles and their models.
- **Objective 5**: Design a simulator and a FPGA emulator for the new architecture (CIM device combined with a conventional CPU)

European Commission

**MNEMOSENE** has received funding from the European Union's Horizon 2020 research and innovation programme under the ICT-31-2017 RIA grant agreement No 780215

# Overall Approach

To achieve the project targets, a solid strategy has been set up that divides the needed work into four main interrelated components.




European Commission

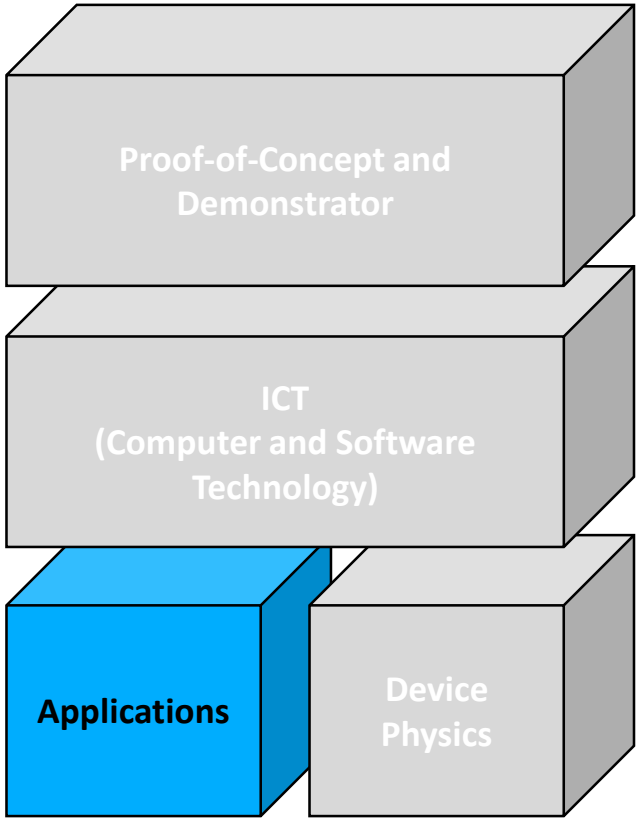
**MNEMOSENE** has received funding from the European Union's Horizon 2020 research and innovation programme under the ICT-31-2017 RIA grant agreement No 780215

# Overall Approach

**Applications**: Analysis of the requirements and existing implementations of specific applications; development of suitable new solutions for the proposed architecture.

Targeted applications include:

- healthcare/genomics;
- data sciences / matrix vector multiplications;
- database / bitmap index; and
- IoT applications / ultra-low-power sensor-node processing
- image and video processing

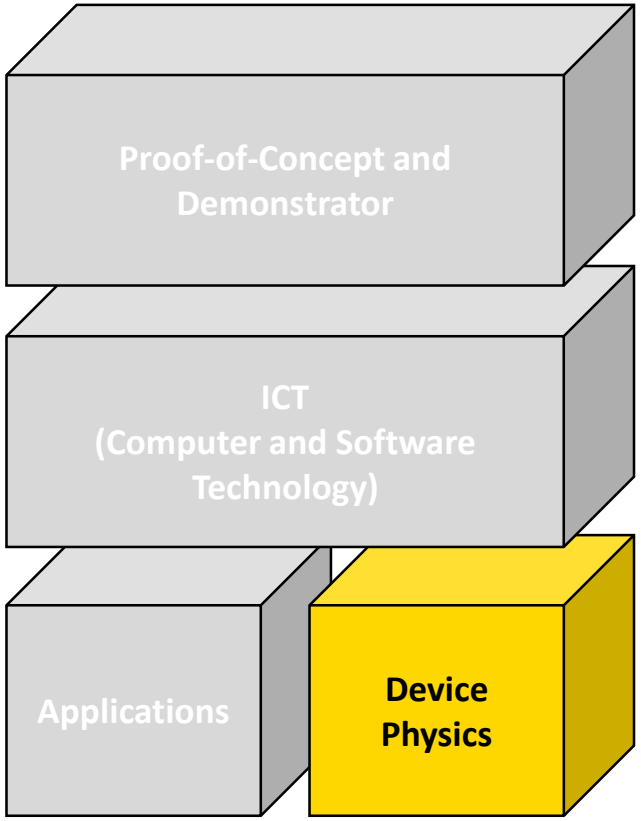



European Commission

**MNEMOSENE** has received funding from the European Union's Horizon 2020 research and innovation programme under the ICT-31-2017 RIA grant agreement No 780215

# Overall Approach

**Device Physics**: Investigation of the properties of new materials in order to recommend the best device (and device models) suitable for the implementation of the targeted CIM architecture; fabrication, characterization and modelling of devices.




European Commission

**MNEMOSENE** has received funding from the European Union's Horizon 2020 research and innovation programme under the ICT-31-2017 RIA grant agreement No 780215

# Overall Approach

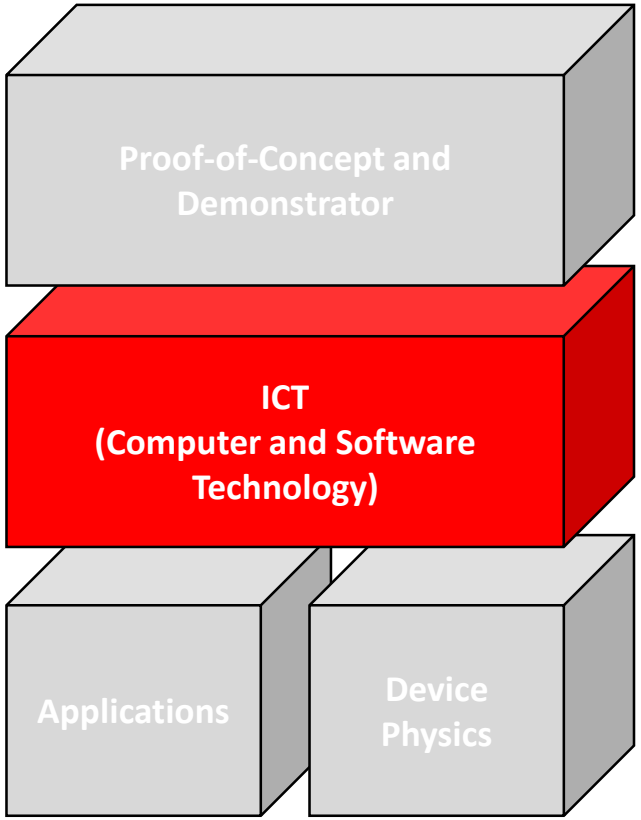
**ICT (Computer and Software Technology)**:

Hardware level:

- Macro-architecture exploration: integration of multiple CIM tiles, overall scheduling of the operation, optimisation of communications and interconnects.
- Micro-architecture exploration: development and implementation of primitive functions (logic and arithmetic)

Software level:

- Design space exploration and efficient mapping of C programs on the CIM architecture for the targeted applications

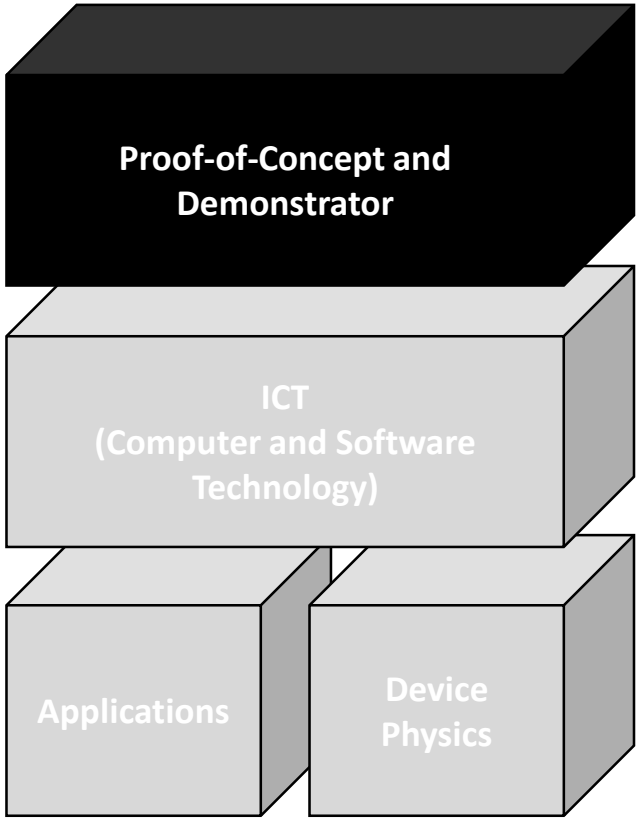



European Commission

**MNEMOSENE** has received funding from the European Union's Horizon 2020 research and innovation programme under the ICT-31-2017 RIA grant agreement No 780215

# Overall Approach

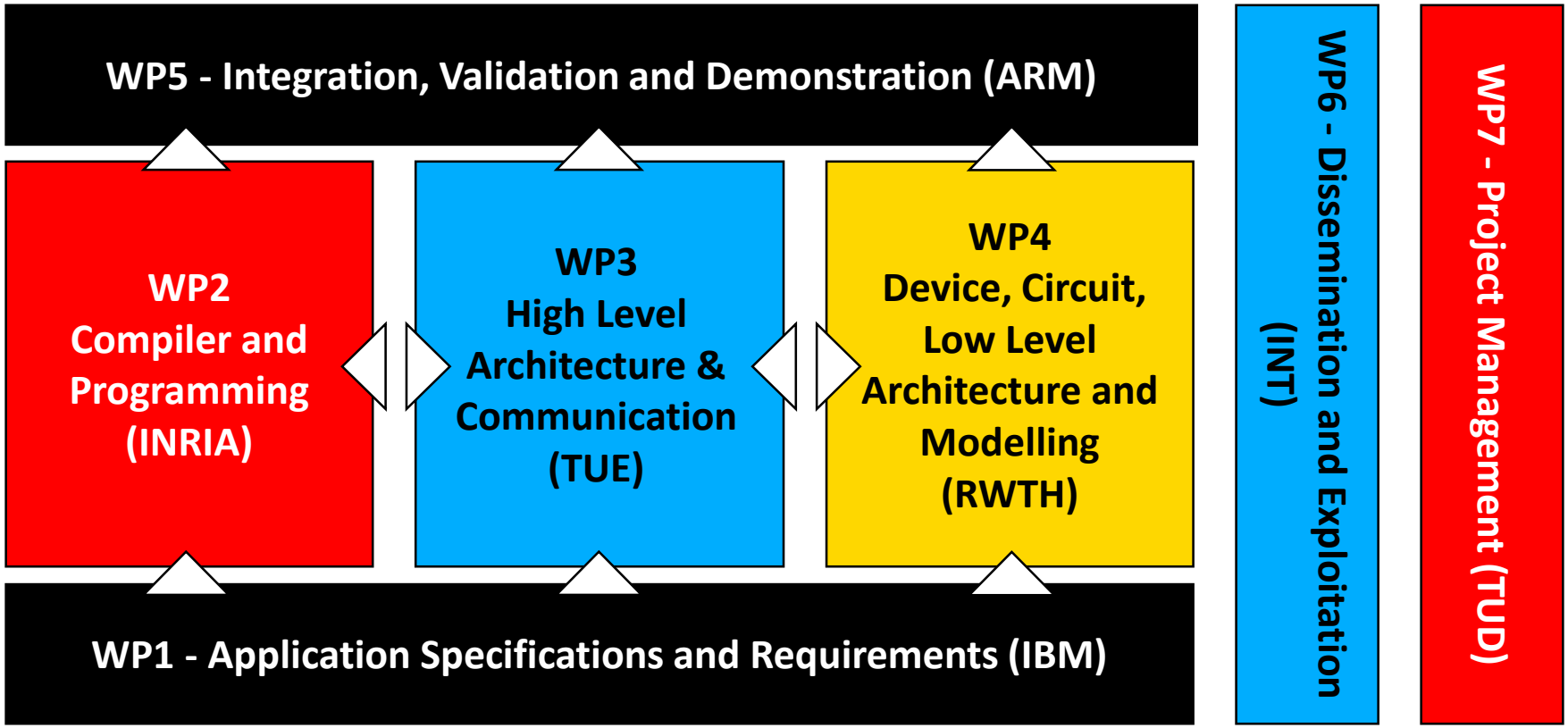
**Proof-of-Concept and Demonstrator**: Demonstration of the architecture concept by using fabricated basic building blocks (consisting of small crossbar arrays) and a CMOS interconnect fabric integrated on a PCB board to mimic a monolithic integration. Demonstration of the full MNEMOSENE architecture (conventional CPU - CIM die) based on simulation (using calibrated basic models) and emulation (using FPGAs).




European Commission

**MNEMOSENE** has received funding from the European Union's Horizon 2020 research and innovation programme under the ICT-31-2017 RIA grant agreement No 780215

# Workplan




European Commission

**MNEMOSENE** has received funding from the European Union's Horizon 2020 research and innovation programme under the ICT-31-2017 RIA grant agreement No 780215

# Expected Impacts

- Transform computer science into using new **highly parallel CIM architectures and technologies**.
- Drive silicon technology into using **new memristor based devices and circuits**.
- Realize **significant improvements in computing energy and area efficiency** compared to other domain specific solutions (at least 5x) and general purpose architectures (up to 100-1000x).
- Enable computation of currently unfeasible **big data applications** with important societal consequences
- Enable novel applications towards **low power electronics**.
- Support breakthrough development in **Neuromorphic Computing** and **Quantum Computing**.

European Commission

**MNEMOSENE** has received funding from the European Union's Horizon 2020 research and innovation programme under the ICT-31-2017 RIA grant agreement No 780215

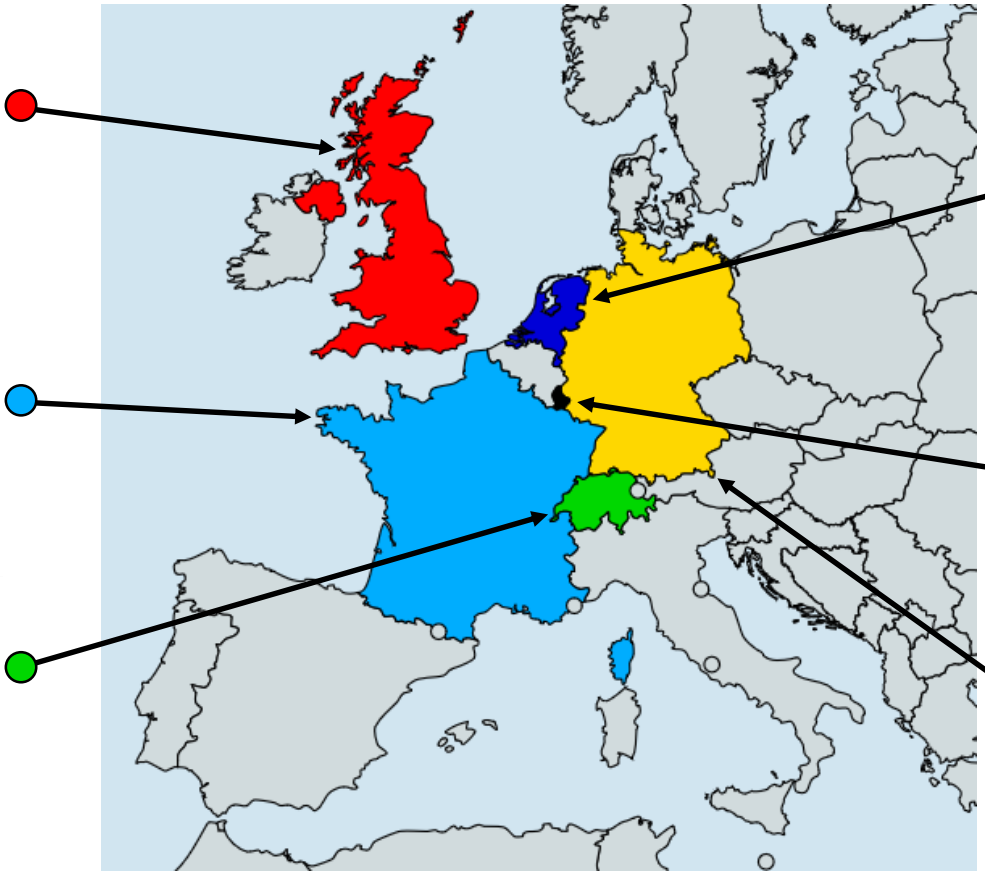
# Consortium

arm

Inria
INVENTEURS DU MONDE NUMÉRIQUE

ETH zürich

IBM Research



TU Delft

TU/e Technische Universiteit Eindhoven University of Technology
Where innovation starts

imec

intelligentsia consultants

RWTH AACHEN UNIVERSITY

European Commission

**MNEMOSENE** has received funding from the European Union's Horizon 2020 research and innovation programme under the ICT-31-2017 RIA grant agreement No 780215

# Contact Information

## Project Coordinator

**Prof. Said HAMDIOUI**

Technische Universiteit Delft - Department of Quantum and Computer Engineering (TUD)

Tel.: (+31) 15 27 83643

Email: s.hamdioui@tudelft.nl

http://www.ce.ewi.tudelft.nl/

**www.mnemosene.eu**

European Commission

**MNEMOSENE** has received funding from the European Union's Horizon 2020 research and innovation programme under the ICT-31-2017 RIA grant agreement No 780215