MNEMOSENE
computation-in-memory architecture based on resistive devices

Newsletter No. 4
July 2020 - June 2021
www.mnemosene.eu

MNEMOSENE comes to completion

MNEMOSENE has been an ambitious research and innovation action addressing the theme "*Development of new approaches to scale functional performance of information processing and storage substantially beyond the state-of-the-art technologies with a focus on ultra-low power and high performance*" of the EU's Horizon 2020 ICT research and innovation programme. The project last 3,5 years and was funded with a total of 4M €. Coordinated by Prof. Said Hamdioui at Delft Technical University (NL), the MNEMOSENE Consortium included Eindhoven University of Technology and IMEC (NL), ETH Zurich and IBM Research – Zurich (CH), Arm (UK), RWTH Aachen University (DE), INRIA (FR) and Intelligentsia Consultants (LU).

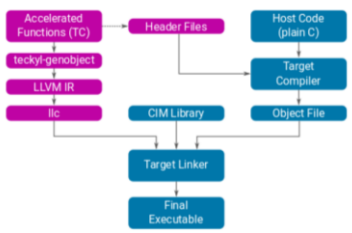
To meet the requirements of future electronic applications, MNEMOSENE focused on the development, design and demonstration of a Computation-In-Memory (CIM) architecture based on extending arrays of non-volatile resistive switching devices (memristors) with logic functionality inside or around the cell array.

In this final MNEMOSENE newsletter, we highlight some of the important final results that were reported as well as peer-review journal articles and conference papers that were published. Reflecting the project's success, we are also proud to bring news of prizes won by the consortium and by individual project members based on MNEMOSENE research.

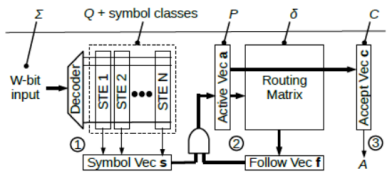
News

02.07.2020, Report published on mapping common micro-kernels to realistic digital applications Prepared by MNEMOSENE consortium partner ETH Zurich, the report explains the process and initial experimental results of mapping common micro-kernels to realistic digital applications (e.g. database, image processing and IoT sensory), which have been enhanced using in-memory computing accelerators.

30.08.2020, Report published on the final compilation infrastructure The report describes the final version of the parallelizing compiler for the Computation-in-Memory (CIM) architecture developed in the project. Created by MNEMOSENE consortium partner INRIA, the compiler allows for the compilation of high-level representations of critical operations of target applications for the CIM architecture with a simplified and extensible compilation flow.



12.10.2020, Final report published on new algorithmic solutions Prepared by TU Delft, the report provides the final algorithmic solutions developed for database query, matching with automata processor, guided image filtering, deep learning inference, and hyper-dimensional computing applications.



European Commission

The MNEMOSENE project has received funding from the European Union's Horizon 2020 Research and Innovation Programme under grant agreement No 780215.

News (continued)

26.11.2020, MNEMOSENE project announced the winner of the European Commission's ECS Innovation Award for EFECS 2020!

The MNEMOSENE project was chosen the winner of the European Commission's prestigious ECS Innovation Award for EFECS 2020. The ECS Innovation Award is a prize given annually by the Competitive Electronics Industry's unit of the European Commission's Directorate-General for Communications Networks, Content and Technology. The prize is awarded to the most innovative idea developed under a Horizon 2020 project in the field of Electronic Components and Systems (ECS). Notably, the competition aims to promote the richness of the technology developed in the ECS area and the significant importance that it has for the EU economy and citizens.

The ECS Innovation Award was presented to Professor Said Hamdioui, MNEMOSENE's Project Coordinator, at a dedicated session of the European Forum for Electronic Components and Systems (EFECS 2020). During his award acceptance speech, Prof. Hamdioui presented how MNEMOSENE's innovative developments in computation-in-memory (CIM) architecture based on memresistor devices will lead to 10X to 100X factor improvements in energy efficiency and performance efficiency of computers. In turn, this will enable cost effective computation of currently unfeasible artificial intelligence applications, support breakthrough development in neuromorphic computing, and position Europe in a leading role in unconventional computer architectures and memristive technology.

4.1.2021, Reports published on refined memristor crossbar-based logic and memory design and models as well as refined CIM microarchitecture

The first report covers the refined memristor crossbar-based logic and memory design and models. Led by IMEC, the report investigates, on the lowest hardware level, the impact of memristor array architecture and analogue/digital converter (ADC) design choices on the performance of multiply-and-accumulate (MAC) operations for Resistive Random-Access Memories (ReRAM) based memsristor devices.

The second report covers the refined CIM microarchitecture. Led by IMEC, the report presents the work done to further refine the CIM tile architecture, adapt the CIM simulator accordingly, present more detailed performance and energy results, and demonstrate how the design-space exploration can be performed using the CIM simulator.

European Commission

The MNEMOSENE project has received funding from the European Union's Horizon 2020 Research and Innovation Programme under grant agreement No 780215.

News (continued)

5.2.2021, Congratulations to Jintao Yu on his PhD graduation!

Our congratulations to Jintao Yu on his PhD graduation at TU Delft. The title of his PhD thesis is "Computation-in-Memory: From Circuits to Compilers" and is partly based on research conducted during the MNEMOSENE project.

12.2.2021, PhD student Abhairaj Singh a winner of a 2021 IBM PhD Fellowship Award!

PhD student Abhairaj Singh - a research student of Prof. Said Hamdioui working on the MNEMOSENE project - was announced one of 16 winners of a 2021 IBM PhD Fellowship Award.

PhD student Abhairaj Singh

For 70 years IBM has recognized and rewarded outstanding PhD students around the world through a highly competitive IBM PhD Fellowship Award program. The distinguished 2021 IBM PhD Fellowship Award recipients demonstrated expertise in pioneering research areas, such as artificial intelligence, hybrid cloud technology, quantum computing, data science, security, and the next generation of cutting-edge processors.

8.4.2021, Prof. Said Hamdioui gives IEEE Circuits and Systems (CAS) distinguished lecture

Prof. Said Hamdioui gave a well received lecture on "*Computation-in-Memory Architectures for Edge-AI*" as part of the IEEE Circuits and Systems' (CAS) Distinguished Lecture Programme (DLP).

Prof. Said Hamdioui

CAS is the leading organization that promotes the advancement of the theory, analysis, design, tools, and implementation of circuits and systems. The field spans their theoretical foundations, applications, and architectures, as well as circuits and systems implementation of algorithms for signal and information processing.

European Commission

The MNEMOSENE project has received funding from the European Union's Horizon 2020 Research and Innovation Programme under grant agreement No 780215.

Publications

In the period between July 2020 and June 2021, research supported by MNEMOSENE has resulted in numerous publications in peer-reviewed journals and conference proceedings:

[1] S. Wiefels, C. Bengal, N. Kopperberg, K. Zhang, R. Waser, S. Menzel, "*HRS Instability in Oxide-Based Bipolar Resistive Switching Cells*", in IEEE Transactions on Electron Devices, DOI: 10.1109/TED.2020.3018096.

[2] M. Zahedi, M. Mayahinia, M. Abu. Lebdeh, S. Wong, S. Hamdioui, "*Efficient Organization of Digital Periphery to Support Integer Datatype for Memristor-Based CIM*", in 2020 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), DOI: 10.1109/ISVLSI49217.2020.00047.

[3] G. Karunaratne, M. Le Gallo, G. Cherubini, L. Benini, A. Rahimi, A. Sebastian, "*In-memory hyperdimensional computing*", in Nature Electronics, DOI: 10.1038/s41928-020-0410-3.

[4] I. Giannopoulos, A. Singh, M. Le Gallo, V.P. Jonnalagadda, S. Hamdioui, and A. Sebastian, "*In-memory database query*", in Advanced Intelligent Systems, DOI: 10.1002/aisy.202000141.

[5] C. Bengel, A. Siemon, F. Cüppers, S. Hoffmann-Eifert, A. Hardtdegen, M. von Witzleben, L. Hellmich, R. Waser, S. Menzel, "*Variability-Aware Modeling of Filamentary Oxide-Based Bipolar Resistive Switching Cells Using SPICE Level Compact Models*", in IEEE Transactions on Circuits and Systems I: Regular Papers, DOI: 10.1109/TCSI.2020.3018502.

[6] A. BanaGozar, K. Vadivel, J. Multanen, P. Jääskeläinen, S. Stuijk, H. Corporaal, "*System Simulation of Memristor Based Computation In Memory Platforms*", in Proceedings of International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation.

[7] A. Drebes, L. Chelini, O. Zinenko, A. Cohen, H. Corporaal, T. Grosser, K. Vadivel, N. Vasilache, "*TC-CIM: Empowering Tensor Comprehensions for Computing-In-Memory*", in Proceedings of 10th International Workshop on Polyhedral Compilation Techniques.

[8] K. Vadivel, L. Chelini, A. BanaGozar, G. Singh, S. Corda, R. Jordans, H. Corporaal, "*TDO-CIM: transparent detection and offloading for computation in-memory*", in Proceedings of DATE 2020, DOI: 10.23919/DATE48585.2020.9116464.

[9] K. Komisarczyk, L. Chelini, K. Vadivel, R. Jordans, H. Corporaal, "*PET-to-MLIR: A polyhedral front-end for MLIR*", in Proceedings of 23rd Euromicro Conference on Digital System Design, DOI: 10.1109/DSD51259.2020.00091.

[10] F. García-Redondo, S. Das, G. Rosendale, "*Training DNN IoT Applications for Deployment On Analog NVM Crossbars*", in Proceedings of 2020 International Joint Conference on Neural Networks (IJCNN), DOI: 10.1109/IJCNN48605.2020.9206822.

[11] A. Singh, M. A. Lebdeh, A. Gebregiorgis, R. Bishnoi, R. V. Joshi, S. Hamdioui, "*SRIF: Scalable and Reliable Integrate and Fire Circuit ADC for Memristor-Based CIM Architectures*", in Transactions in Circuits and Systems-I (TCAS1), DOI: 10.1109/TCSI.2021.3061214.

[12] A. Singh, S. Diware, A. Gebregiorgis, R. Bishnoi, F. Catthoor, R. V. Joshi, Said Hamdioui, "*Low-power Memristor-based Computing for Edge-AI Applications*", in Proceedings of International Symposium on Circuit and Systems (ISCAS 2021), DOI: 10.1109/ISCAS51556.2021.9401226.

European Commission

The MNEMOSENE project has received funding from the European Union's Horizon 2020 Research and Innovation Programme under grant agreement No 780215.

Publications (continued)

[13] M. Fieback, S. Nagarajan, R. Bishnoi, M. Tahoori, M. Taouil, S. Hamdioui, "*Testing Scouting Logic-Based Computation-in-Memory Architectures*", in Proceedings of 2020 IEEE European Test Symposium (ETS), DOI: https://doi.org/10.1109/ETS48528.2020.9131604.

[14] C. Bengel, A. Siemon, V. Rana, S. Menzel, "*Implementation of Multinary Lukasiewicz Logic using Memristive Devices*", in Proceedings of International Symposium on Circuit and Systems (ISCAS 2021).

[15] C. Bengel, F.Cüppers, M. Payvand, R. Dittmann, R. Waser, S. Hoffmann-Eifert, S. Menzel, "*Utilizing the Switching Stochasticity of HfO2/TiOx-Based ReRAM Devices and the Concept of Multiple Devices for the Classification of Overlapping and Noisy Patterns*", in Frontiers in Neuroscience.

[16] S. Menzel, C. Bengel, J. Mohr, S. Wiefels, F. Cüppers , S. Hoffmann-Eifert, D. Wouters, "*Reliability Aspects of Memristive Devices for Computation-in-Memory Applications*", in Proceedings of International Workshop on Cellular Nanoscale Networks and their Applications (CNNA 2021).

[17] F. Garcia Redondo, K. Vadivel, S. Das, A. Banagozar, H. Corporaal, "*SACA: System-level Simulation Framework Integrating Non-Ideal Analog CIM Accelerators*", in Proceedings of 54th IEEE/ACM International Symposium on Microarchitecture.

[18] M. Mayahinia, A. Singh, C. Bengel, S. Wiefels, M. A. Lebdeh, S. Menzel, D.J. Wouters, A. Gebregiorgis, R. Bishnoi, R. Joshis, and S. Hamdioui, "*A Voltage Controlled Oscillation based ADC Design for Computation-in-Memory Architectures Using Emerging ReRAMs*", in Journal in Emerging Technologies in Computing Systems (JETC).

Last but not least …

17.2.2021, Prof. Said Hamdioui a keynote speaker at Workshop on Interdependent Challenges of Reliability, Securty and Quality (RESCUE 2021)

Prof. Said Hamdioui made a keynote address on "Re-engineering Test and Reliability for Emerging Computing Technologies" during the recent Workshop on Interdependent Challenges of Reliability, Securty and Quality (RESCUE 2021) held in conjunction with the Design, Automation and Test in Europe Conference (DATE 21).

2.3.2021, Prof. Said Hamdioui gives keynote address at 34th International Conference on VLSI Design and the 20th International Conference on Embedded Systems (VLSID 2021)

"Design and Test of Computing Architectures for Edge AI: Opportunities and Challenges" was the title of Prof. Said Hamdioui's recent keynote address at the 34th International Conference on VLSI Design and the 20th International Conference on Embedded Systems (VLSID 2021).

Contact

Prof. Said Hamdioui
(Project Coordinator)

Technische Universiteit Delft, Department of Computer Engineering
Mekelweg 4, 2628CD Delft (NL)
s.hamdioui@tudelft.nl

European Commission

The MNEMOSENE project has received funding from the European Union's Horizon 2020 Research and Innovation Programme under grant agreement No 780215.