MNEMOSENE
computation-in-memory architecture
based on resistive devices

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MNEMOSENE at a glance

MNEMOSENE is an ambitious research and innovation action addressing the theme "*Development of new approaches to scale functional performance of information processing and storage substantially beyond the state-of-the-art technologies with a focus on ultra-low power and high performance*" of the EU's Horizon 2020 ICT research and innovation programme. The project will last 3 years and has been funded with a total of 4M €. Coordinated by Said Hamdioui at Delft Technical University (NL), the MNEMOSENE Consortium include Eindhoven University of Technology and IMEC (NL), ETH Zurich and IBM Research – Zurich (CH), Arm (UK), RWTH Aachen University (DE), INRIA (FR) and Intelligentsia Consultants (LU).

In order to meet the requirements of future electronic applications, MNEMOSENE will focus on the development, design and demonstration of a Computation-In-Memory (CIM) architecture based on extending arrays of non-volatile resistive switching devices (memristors) with logic functionality inside or around the cell array.

MNEMOSENE officially started in January 2018 and has now successfully concluded 30 months of activities. Important results have been achieved and disseminated through peer-review publications and participation to conferences and seminars.

News

25.09.2019, Successful MNEMOSENE Midterm Review The MNEMOSENE consortium held a successful midterm review meeting in early September 2019 with the EC project officer and two project monitors. The consortium was pleased to hear that the project was assessed to have fully achieved its objectives and milestones during its first 18 months. Furthermore, the project was considered as progressing appropriately with a good level of dissemination and published papers.

22.01.2020, Partners present results at HiPEAC 2020 MNEMOSENE partners presented three papers at the HiPEAC 2020 conference in Bologna:

Declarative Loop Tactics for Domain-Specific Optimization
https://dl.acm.org/doi/abs/10.1145/3372266

Flextended Tiles: A Flexible Extension of Overlapped Tiles for Polyhedral Compilation
https://dl.acm.org/doi/abs/10.1145/3369382

The Next 700 Accelerated Layers: From Mathematical Expressions of Network Computation Graphs to Accelerated GPU Kernels Automatically
https://dl.acm.org/doi/abs/10.1145/3355606

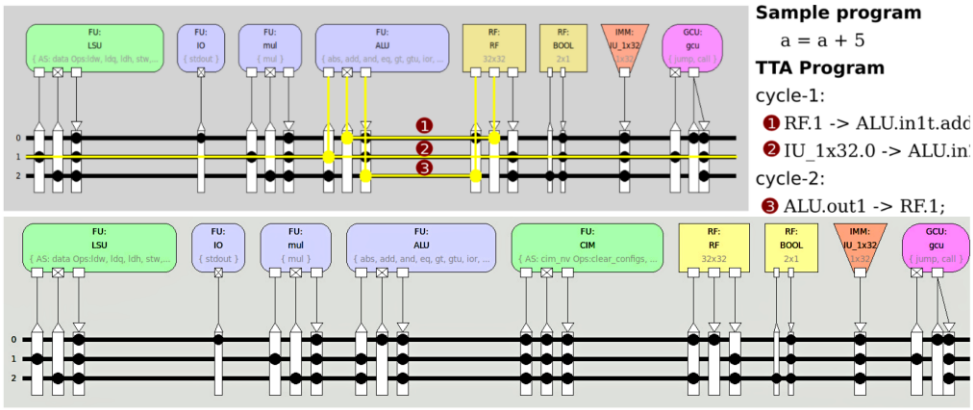
European Commission

The MNEMOSENE project has received funding from the European Union's Horizon 2020 Research and Innovation Programme under grant agreement No 780215.

News (continued)

20.04.2020, Refined Computation-in-Memory Architecture

The MNEMOSENE consortium published the final specification for the instruction set architecture (ISA) for the whole computation-in-memory (CIM) architecture as well as the results of preliminary performance tests. Over the past two years, TU Eindhoven has been leading the consortium's development of a macro Non-Von Neumann architecture and its CIM-ISA to support storage and computation in the same physical location. So far, tests to evaluate the CIM units using a low-power transport triggered architecture (TTA) have demonstrated major improvements in performance (up to 3.9X faster), energy consumption (up to 69% lower), and combined energy, delay, area product (EDAP) (up to 84% lower).



TTA based processors overview. LoTTA (Top). LoTTA+1×CIM (Bottom)

01.06.2020, MNEMOSENE consortium partners publish authoritative research paper about *In-Memory Hyperdimensional Computing* in *Nature Electronics*

Based on results from the MNEMOSENE project, IBM Research and ETH Zurich have published an authoritative research paper about *In-Memory Hyperdimensional Computing* in the prestigious journal *Nature Electronics*. In the paper, the partners report a complete in-memory hyperdimensional computing system in which all operations are implemented on two memristive crossbar engines together with peripheral digital complementary metal–oxide–semiconductor (CMOS) circuits. Their approach can achieve a near optimum trade-off between design complexity and classification accuracy based on three prototypical hyperdimensional computing related learning tasks: language classification, news classification, and hand gesture recognition from electromyography signals. Experiments using 760,000 phase-change memory devices performing analogue in-memory computing have achieved comparable accuracies to software implementations.

- To read the full paper, please click on the following link.
- To watch an accompanying video, please click on the following link.
- To read a related IBM blog article, please click on the following link.

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News (continued)

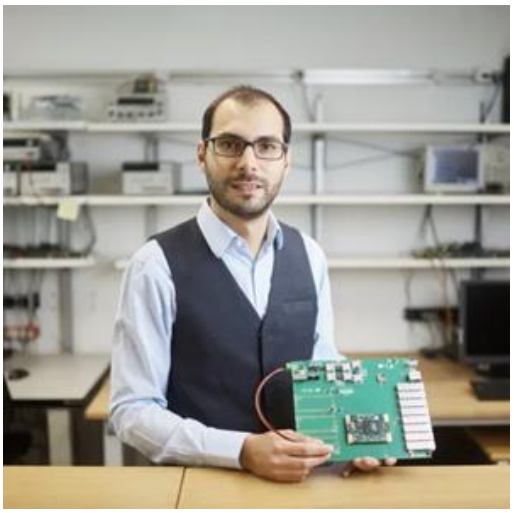
25.04.2020, Welcome to a new team member!

The MNEMOSENE consortium was pleased to welcome to their team the new member, Dr. Anteneh Gebregiorgis. Dr. Gebregiorgis recently joined TU Delft where he will be supporting the MNEMOSENE project coordinator, Prof. Said Hamdioui, with managing and organising the project's workflow. Prior to his arrival, Dr. Gebregiorgis received his PhD degree in Computer Science from Karlsruhe Institute of Technology where he also worked as a postdoctoral researcher on hardware design for neuromorphic systems.

Dr. Anteneh Gebregiorgis

22.06.2020, Dr. Manuel Le Gallo named one of MIT Technology Review's 35 innovators under 35 2020!

Dr. Manuel Le Gallo of IBM Research - and a key expert in the MNEMOSENE project – has been named one of *MIT Technology Review's 35* innovators under 35 2020. Being selected a top young innovator in *MIT Technology Review*'s annual list is a highly prestigious honour. The list has been compiled for the past 20 years and the contest attracts over 500 nominations each year. Dr. Le Gallo was chosen in the category "Inventor" for his work on Computation-in-Memory using memristive devices, which is also the focus of the MNEMOSENE project. This key enabling technology will help to make artificial intelligence programmes less power consuming to run on computers.



Dr. Manuel Le Gallo
(Photo credit: Samuel Trümpy)

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Publications

In the period between July 2019 and June 2020, research supported by MNEMOSENE has resulted in the following publications in peer-reviewed journals and conference proceedings:

[1] A. Burrello, K. A. Schindler, L. Benini, A. Rahimi, *"Hyperdimensional Computing with Local Binary Patterns: One-shot Learning for Seizure Onset Detection and Identification of Ictogenic Brain Regions from Short-time iEEG Recordings"*, in IEEE Transactions on Biomedical Engineering. DOI: 10.1109/TBME.2019.2919137

[2] N. Vasilache, O. Zinenko, T. Theodoridis, P. Goyal, Z. Devito, W. S. Moses, S. Verdoolaege, A. Adams, A. Cohen, *"The Next 700 Accelerated Layers: From Mathematical Expressions of Network Computation Graphs to Accelerated GPU Kernels, Automatically"*, in ACM Transactions on Architecture and Code Optimization, DOI: 10.1145/3355606

[3] J. Zhao, A. Cohen, *"Flextended Tiles: a Flexible Extension of Overlapped Tiles for Polyhedral Compilation"*, in ACM Transactions on Architecture and Code Optimization, DOI: 10.1145/3369382

[4] H. A. D. Nguyen, J. Yu, M. A. Lebdeh, M. Taouil, S. Hamdioui, *"A computation-in-memory accelerator based on resistive devices"*, in Proceedings of the International Symposium on Memory Systems - MEMSYS '19, DOI: 10.1145/3357526.3357554

[5] M. Douthwaite, F. Garcıa-Redondo, P. Georgiou and S. Das, *"A Time-Domain Current-Mode MAC Engine for Analogue Neural Networks in Flexible Electronics"*, in Proceedings of the 2019 IEEE Biomedical Circuits and Systems Conference (BioCAS), DOI: 10.1109/BIOCAS.2019.8919190

[6] M. Hersche, S. Sangalli, L. Benini, A. Rahimi, *"Evolvable Hyperdimensional Computing: Unsupervised Regeneration of Associative Memory to Recover Faulty Components"*, in Proceedings of the 2nd IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS 2020), Genoa, Italy. DOI: 10.3929/ethz-b-000387115

[7] M. Hersche, L. Benini, A. Rahimi, *"Binary Models for Motor-Imagery Brain–Computer Interfaces: Sparse Random Projection and Binarized SVM"*, in Proceedings of the 2nd IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS 2020), Genoa, Italy. DOI: 10.3929/ethz-b-000387116

[8] M. Hersche, P. Rupp, L. Benini, A. Rahimi, *"Compressing Subject-specific Brain–Computer Interface Models into One Model by Superposition in Hyperdimensional Space"*, in Proceedings of the 2020 ACM/IEEE Design, Automation and Test in Europe (DATE 2020), Grenoble, France. DOI: 10.3929/ethz-b-000387115.

[9] B. Hoffer, V. Rana, S. Menzel, R. Waser, S. Kvatinsky, *"Experimental Demonstration of Memristor-Aided Logic (MAGIC) Using Valence Change Memory (VCM)"*, in IEEE Transactions on Electron Devices, DOI: 10.1109/TED.2020.3001247

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